CLAIMS

What is claimed is:

1. A method of forming a dielectric structure for a flash memory cell, the method comprising:

forming a first layer of silicon dioxide;

forming a silicon nitride layer on the first layer of silicon dioxide;

pretreating the silicon nitride layer including oxidizing the silicon nitride; and

depositing a second layer of silicon dioxide on the pretreated silicon nitride layer.

2. The method of claim 1, wherein oxidizing the silicon nitride occurs in a batch furnace at a temperature of approximately 800°C to 1050°C for approximately 5 min. to 15 min.

3. The method of claim 2, wherein oxidizing the silicon nitride occurs at a pressure of approximately 1 atm. to 10 atm.

4. The method of claim 2, wherein oxidizing the silicon nitride occurs with a gas mixture of approximately 5% oxygen to 100% oxygen.

5. The method of claim 2, wherein oxidizing the silicon nitride occurs with a gas mixture of approximately 5% steam to 100% steam.

6. The method of claim 1, wherein oxidizing the silicon nitride occurs in a single wafer tool at a temperature of approximately 800°C to 1100°C for approximately 0.1 s to 6 s.

7. The method of claim 6, wherein oxidizing the silicon nitride occurs at a pressure of approximately 1 atm. to 10 atm.

8. The method of claim 6, wherein oxidizing the silicon nitride occurs with a gas mixture of approximately 5% oxygen to 100% oxygen.

9. The method of claim 6, wherein oxidizing the silicon nitride occurs with a gas mixture of approximately 1% steam to 10% steam.

10. A method of making a flash memory cell including a substrate, a tunnel oxide and a first polysilicon layer, the method comprising:

forming a first layer of silicon dioxide on the first polysilicon layer;

forming a silicon nitride layer nitride on the first layer of silicon dioxide;

pretreating the silicon nitride layer including oxidizing the silicon nitride; and

depositing a second layer of silicon dioxide on the pretreated silicon nitride layer.

11. The method of claim 10, wherein oxidizing the silicon nitride occurs in a batch furnace at a temperature of approximately 800°C to 1050°C for approximately 5 min. to 15 min. with a gas mixture of approximately 5% oxygen to 100% oxygen and a diluent, the diluent comprising one of argon and nitrogen.

12. The method of claim 10, wherein oxidizing the silicon nitride occurs in a batch furnace with a temperature of approximately 800°C to 1050°C for approximately 5 min. to 15 min. with a gas mixture of approximately 5% steam to 100% steam and a diluent, the diluent comprising one of argon and nitrogen.

13. The method of claim 10, wherein oxidizing the silicon nitride occurs in a single wafer tool at a temperature of approximately 800°C to 1100°C for approximately 0.1 s to 6 s with a gas mixture of approximately 5% oxygen to 100% oxygen and a diluent, the diluent comprising one of argon and nitrogen.

14. The method of claim 10, wherein oxidizing the silicon nitride occurs in a single wafer tool at a temperature of approximately 800°C to 1100°C for approximately 0.1 s to 6 s with a gas mixture of approximately 1% steam to 10% steam and a diluent, the diluent comprising one of argon and nitrogen.

15. The method of claim 10, wherein the first layer of silicon dioxide is approximately 40Å to 70Å thick, the silicon nitride layer is approximately 50Å to 150Å thick, and the second layer of silicon dioxide is approximately 30Å to 50Å thick.

16. The method of claim 10, further comprising forming a second polysilicon layer on the second layer of silicon dioxide.

17. A flash memory cell comprising:

a tunnel oxide;

a first polysilicon layer formed on the tunnel oxide;

a second polysilicon layer disposed a predetermined distance above the first polysilicon layer; and

an ONO structure disposed between the first and second polysilicon layers, the ONO structure comprising:

a first oxide layer;

a nitride layer formed on the first oxide layer; and

a second oxide layer deposited on the nitride layer,

wherein the nitride layer has been oxidized prior to deposition of the second oxide layer.

18. The memory cell of claim 17, wherein the nitride layer is oxidized in a batch furnace at a temperature of approximately 800°C to 1050°C for approximately 5 min. to 15 min. with a gas mixture of approximately 5% to 100% oxygen and a diluent, the diluent comprising one of argon and nitrogen.

19. The memory cell of claim 17, wherein the nitride layer is oxidized in a batch furnace at a temperature of approximately 800°C to 1050°C for approximately 5 min. to 15 min. with a gas mixture of approximately 5% to 100% steam and a diluent, the diluent comprising one of argon and nitrogen.

20. The memory cell of claim 17, wherein the nitride layer is oxidized in a single wafer tool at a temperature of approximately 800°C to 1100°C for approximately 0.1 s to 6 s with a gas mixture of approximately 5% to 100% oxygen and a diluent, the diluent comprising one of argon and nitrogen.

21. The memory cell of claim 17, wherein the nitride layer is oxidized in a single wafer tool at a temperature of approximately 800°C to 1100°C for approximately 0.1 s to 6 s with a gas mixture of approximately 1% to 10% steam and a diluent, the diluent comprising one of argon and nitrogen.